REMARKS

Claims 1-20 are all the claims pending in the application.

Claims 1-20 have been amended to better conform them to U.S. patent practice and to further clarify the claimed invention.

Applicant notes that the Examiner has not indicated whether the drawings are accepted or objected to. Applicant requests that the Examiner indicate that the drawings are accepted in the next office action.

35 U.S.C. § 101 Rejections

The Examiner has rejected claim 16-20 under 35 U.S.C. § 101 as allegedly being directed to non-statutory subject matter. Applicant has amended the claims as suggested by the Examiner. Therefore, the Examiner is requested to withdraw the §101 rejections.

Prior Art Rejections

The Examiner has rejected claims 8-20 under 35 U.S.C. § 102(b) as being anticipated by Klug (U.S. Patent No. 5,226,152). Applicant traverses these rejections because Klug fails to disclose or suggest all of the limitations of the claims, as amended. Specifically, Klug fails to disclose or suggest at least the following limitations of claims 8 and 16:

> checking if first and second sequences of I/O transactions addressed to said device controller issued from said first and second CPU modules, respectively, match and determining whether out-of synchronization occurs.

Generally, when first and second CPU modules issue respective sequences of the I/O transactions to the device controllers, each of the respective sequences includes the I/O transactions addressed to one device controller and another. As shown in figure 2, as an example only, the order of one I/O instruction (IO-B1) to one device controller and another I/O

transaction (IO-A2) to another device controller may differ between the two sequences. In this c case, the two sequences do not completely match. This affects the conventional art because that checks whether the entire two sequences match. However, in the claimed invention, this is not a problem if the first and second sequences of the I/O transactions addressed to the corresponding device controller match.

On the other hand, Krug discloses a compare logic 15 that compares all I/O transactions issued from the processors (1 though N). The compare logic 15, however, is the only element that receives outputs from the processors (1 through N). Therefore, Krug fails to check each of the sequences individually to determine if out of synchronization occurs.

Claims 9-15 and 17-20 should be allowable at least based on their dependence from claims 8 or 16.

The Examiner has rejected claims 1-7 under 35 U.S.C. § 103(a) as being unpatentable over Klug in view of Suffin (U.S. Patent No. 6,691,225). Applicant traverses these rejections because neither Klug nor Suffin disclose or suggest all of the limitations of the claims, as amended. Specifically, at least the following limitations are not disclosed or suggested:

> a plurality of transaction synchronization controllers, each of which is provided with corresponding one of said device controllers, checks if first and second sequences of I/O transactions addressed to said corresponding device controller issued from said first and second CPU modules, respectively, match, and determines whether out-of-synchronization occurs.

As mentioned above, generally, when first and second CPU modules issue respective sequences of the I/O transactions to the device controllers, each of the respective sequences includes the I/O transactions addressed to one device controller and another. As shown in figure

2, as an example only, the order of one I/O instruction (IO-B1) to one device controller and another I/O transaction (IO-A2) to another device controller may differ between the two sequences. In this c case, the two sequences do not completely match. This affects the conventional art because that checks whether the entire two sequences match. However, in the claimed invention, this is not a problem if the first and second sequences of the I/O transactions addressed to the corresponding device controller match. With the transaction synchronization controllers, the present claimed invention overcomes the problem of the conventional art.

On the other hand, Krug discloses a compare logic 15 that compares all I/O transactions issued from the processors (1 though N). The compare logic 15, however, is the only element that receives outputs from the processors (1 through N). Therefore, Krug fails to check each of the sequences individually to determine if out of synchronization occurs.

Suffin discloses a redundant, fault tolerant system which has a plurality of input output controllers 24. The Examiner asserts that the input out controller 24 controller corresponds to an I/O module in the claimed invention. However, Suffin has nothing to do with the transaction synchronization controllers of the claimed invention.

Claims 2-7 should be allowable at least based on their dependence from claim 1.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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